REMARKS

In response to the Official Action of November 12, 2004, claims 53 and 57-59 have been amended in a manner which is believed to overcome the rejection of the claims under prior art and to have claims 57-59 considered with regard to the present examination.

More particularly with regard to paragraph 1 of the Official Action, the Examiner states that claims 57-59 are not considered in Group I because they depend from claim 52, not 53. That was an error and an amendment is hereby made to make these claims each dependent from amended claim 53. As such, they should be considered in Group I.

Referring now to paragraphs 2 and 3 of the Official Action, it is respectfully submitted that claim 53 as amended is neither anticipated nor suggested by US patent 5,699,613, Chong et al (hereinafter Chong). The Examiner states that Chong shows in Figures 6-9 an electronic component to have an electrical component 43 incorporated thereon stating that the electronic component comprises a substrate having at least a front substrate layer 33 for receiving the electrical component 43 as shown in Figure 9. The Examiner goes on to state that the electronic component has conductive vias 38 provided through the substrate or at least a front layer thereof to electrical connection to the electrical component 43, characterised in that the electrical component (should be electronic component) further comprises grooves (as denoted by the Examiner as 24, 26 and 27 in Figure 6) provided in the front surface of the substrate and conductive lines 34 shown in Figures 7b and formed in grooves 24, 26 and 27 for electrical connection to the electrical component 43.

Applicant's attorney respectfully disagrees with this interpretation of Chong. In Chong, the disclosure is directed to a method of manufacturing a multiple layer circuit board with stacked vias having fine dimension and pitch. In the disclosure at column 4, line 62 through column 5, line 43, Figures 6-9 are explained. It is clear that what the Examiner denotes as grooves 24, 26 and 27 are in fact stacked vias as shown in Figure 7 and as explained at column 5, lines 3-5. These vias are not grooves since they are in fact holes. This is clearly explained in

Chong in the text accompanying the description of Figure 4 which illustrates the cross-section of the fabrication process (see column 4, lines 33-48). Specifically, it states at lines 43-46:

> "Given the precision available with photolithographic processing, the holes in dielectric 23 at locations 24, 26, 27, 28 and 29 are nominally 0.12 mm or less in diameter. This is important in that the size and location accuracy of such vias preferably matches the pitch of solder ball arrays of flip-chip die."

The flip-chip die is what the Examiner characterizes as the electrical component 43. Clearly, a via is a hole and in the description in Chong, these holes may be conductive and support solder balls 44 (see Figure 9) which in turn make electrical contact with the flip-chip die 43. Furthermore, the definition of "via" is well-known in the art. Enclosed as Attachment A is an excerpt from http://www.expresspcb.com/ExpressPCBHtm/Tips.htm which gives tips for designing printed circuit boards. In the section entitled "Placing Signal Traces" the second paragraph states:

> "Use vias (also called feed-through holes) to move signals from one layer to the other. A via is a pad with a plated-through hole."

Also, as set forth in Attachment B, which is an excerpt from Xilinx Incorporated, Virtex-4 PCB Designer's Guide dated September 9, 2004, vias are explained at page 10 as follows:

> "A via is a physical piece of metal making an electrical connection between two or more points in the z-space of a PCB. Vias carry signals or power between layers of a PCB. In current plated-through-hole (PTH) technology, a via is formed by plating the inner surface of a hole drilled through the PCB."

It is clear from the enclosed materials, as well as the description set forth in Chong, that the vias shown therein are in fact feed-through holes and are not grooves such as those set forth in amended claim 53 and as disclosed in the application (see Figure 2 of the present application where grooves 6 are clearly shown with associated via apertures 8; see also text at page 12, lines 15-22). It is therefore respectfully submitted that claim 53 is neither disclosed nor suggested by Chong.

What the Examiner characterizes as conductive lines (citing Figure 7, element 34) are in fact plating for facilitating direct solderable connection to various surface mounted electronic components such as the flip-chip die. Specifically, Chong states at column 5, lines 12-15:

> "Conductive polymer fill 37 in the recesses of the upper stacked via plating 34 facilitates direct solderable connection to various surface mounted electronic devices, such as the earlier noted flip-chip die."

A polymor fill in a via is not a conductive line as disclosed and claimed in the present application.

Referring now to paragraphs 4 and 5 of the Official Action, the Examiner rejects claims 54-56 as obvious under 35 U.S.C. §103(a) in view of Chong further in view of US patent 6,031,729, Berkeley et al (hereinafter Berkeley). Berkeley is cited as showing in Figure 4 a ceramic substrate having a front substrate layer 33. In view of the above discussion concerning claim 53, it is respectfully submitted that claims 54-56 are not suggested by Chong further in view of Berkeley since claim 53 is distinguished over the cited art. Similarly, claims 57-59, which now depend from claim 53, are also not suggested by Chong in view of Berkeley in view of claim 53 being distinguished over the cited art.

Referring now to paragraph 6 of the Official Action, the prior art made of record and not relied upon is also not believed to disclose or suggest claim 53 and dependent claims 54-59. None of the references are believed to disclose or suggest an electronic component to have an electrical component incorporated thereon, wherein the electronic component comprises a substrate having at least a front substrate layer with a front face for receiving the electrical component and conductive vias provided through the substrate or at least a front layer thereof for electrical connection to the electrical component, characterized in that the electronic component further comprises grooves provided in the front surface of the substrate, with conductive lines being formed in the grooves for electrical connection to the electrical component.

In view of the foregoing, it is respectfully submitted that the present application as amended is in condition for allowance and such action is earnestly solicited.

Respectfully submitted,

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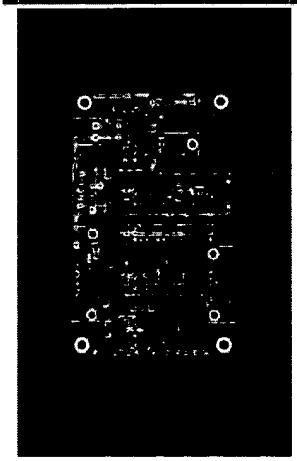


Tips for Designing PCBs

> The engineers at *ExpressPCB* have assembled a few general rules-of-thumb that can help beginners design their first circuit board. These tips are not specific to using our CAD software, but instead provide an overview to help explain how to position the components on the board and how to wire them together.

Placing Components

Generally, it is best to place parts only on the top side of the board.

When placing components, make sure that the *snap-to-grid* is turned on. Usually, a value of 0.050" for the snap grid is best for this job.

First place all the components that need to be in specific locations. This includes connectors, switches, LEDs, mounting holes, heat sinks or any other item that mounts to an external location.

Give careful thought when placing component to minimize trace lengths. Put parts next to each other that connect to each other. Doing a good job here will make laying the traces much easier.

Arrange ICs in only one or two orientations: up or down, and, right or left. Align each IC so that pin one is in the same place for each orientation, usually on the top or left sides.

Position polarized parts (i.e. diodes, and electrolytic caps) with the positive leads all having the same orientation. Also use a square pad to mark the positive leads of these components.

You will save a lot of time by leaving generous space between ICs for traces. Frequently the beginner runs out of room when routing traces. Leave 0.350" - 0.500" between ICs, for large ICs allow even more.

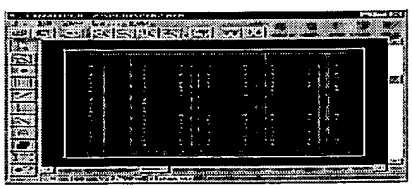
Parts not found in the component library can be made by placing a series of individual pads and then grouping them together. Place one pad for each lead of the component. It is very important to measure the pin spacing and pin diameters as accurately as possible. Typically, dial or digital calipers are used for this job.

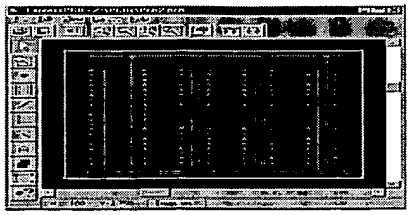
After placing all the components, print out a copy of the layout. Place each component on top of the layout. Check to insure that you have allowed enough space for every part to rest without touching each other.

Placing Power and Ground Traces

After the components are placed, the next step is to lay the power and ground traces. It is essential when working with ICs to have solid power and ground lines, using wide traces that connect to common rails for each supply. It is very important to avoid snaking or daisy chaining the power lines from part-to-part.

One common configuration is shown below. The bottom layer of the PC board is used for both the power and ground traces. A power rail is run along the front edge of the board and a ground rail along the rear edge. From these rails attach traces that run in between the ICs. The ground rail should be very wide, perhaps 0.100", and all the other supply lines should be 0.050". When using this configuration, the remainder of the bottom layer is then reserved for the vertical signal traces.





Placing Signal Traces

When placing traces, it is always a good practice to make them as short and direct as possible.

Use vias (also called feed-through holes) to move signals from one layer to the other. A via is a pad with a plated-through hole.

Generally, the best strategy is to lay out a board with vertical traces on one side and horizontal traces on the other. Add via where needed to connect a horizontal trace to a vertical trace on the opposite side.

A good trace width for low current digital and analog signals is 0.010".

Traces that carry significant current should be wider than signal traces. The table below gives rough guidelines of how wide to make a trace for a given amount of current.

0.010" 0.3 Amps
0.015" 0.4 Amps
0.020" 0.7 Amps
0.025" 1.0 Amps
0.050" 2.0 Amps
0.100" 4.0 Amps
0.150" 6.0 Amps

When placing a trace, it is very important to think about the space between the trace and any adjacent traces or pads. You want to make sure that there is a minimum gap of 0.007" between items, 0.010" is better. Leaving less blank space runs the risk of a short developing in the board manufacturing process. It is also necessary to leave larger gaps when working with high voltage.

When routing traces, it is best to have the *snap-to-grid* turned on. Setting the snap grid spacing to 0.050" often works well. Changing to a value of 0.025" can be helpful when trying to work as densely as possible. Turning off the snap feature may be necessary when connecting to parts that have unusual pin spacing.

It is a common practice to restrict the direction that traces run to horizontal, vertical, or 45 degree angles.

When placing narrow traces, 0.012" or less, avoid sharp right angle turns. The problem here is that in the board manufacturing process, the outside corner can be etched a little more narrow. The solution is to use two 45 degree bends with a short leg in between.

It is a good idea to place text on the top layer of your board, such as a product or company name. Text on the top layer can be helpful to insure that there is no confusion as to which layer is which when the board is manufactured.

Checking Your Work

After all the traces are placed, it is best to double check the routing of every signal to verify that nothing is missing or incorrectly wired. Do this by running through your schematic, one wire at a time. Carefully follow the path of each trace on your PC layout to verify that it is the same as on your schematic. After each trace is confirmed, mark that signal on the schematic with a yellow highlighter.

Inspect your layout, both top and bottom, to insure that the gap between every item (pad to pad, pad to trace, trace to trace) is 0.007" or greater. Use the *Pad Information* tool to determine the diameters of pads that make up a component.

Check for missing vias. *ExpressPCB* will automatically insert a via when changing layers as a series of traces are placed. Users often forget that via are not automatically inserted otherwise. For example, when beginning a new trace, a via is never inserted. An easy way to check for missing via is to first print the top layer, then print the

bottom. Visually inspect each side for traces that don't connect to anything. When a missing via is found, insert one. Do this by clicking on the *Pad* in the side toolbar; select a via (0.056" round via is often a good choice) from the drop down listbox, and click on the layout where the via is missing.

Check for traces that cross each other. This is easily done by inspecting a printout of each layer.

Metal components such as heat sinks, crystals, switches, batteries and connectors can cause shorts if they are placed over traces on the top layer. Inspect for these shorts by placing all the metal components on a printout of the top layer. Then look for traces that run below the metal components.

Virtex-4 PCB Designer's Guide

UG072 (1.1) September 9, 2004

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Vias

A via is a physical piece of metal making an electrical connection between two or more points in the z-space of a PCB. Vias carry signals or power between layers of a PCB. In current plated-through-hole (PTH) technology, a via is formed by plating the inner surface of a hole drilled through the PCB. A via is formed in current microvia technology (also known as High Density Interconnect or HDI) with a laser by ablating the substrate material and deforming the conductive plating, in the process forming a conductive connection. These types of Microvias formed cannot penetrate more than one or two layers, however, they can be stacked or stair-stepped to form vias traversing the full board thickness.

Pads and Anti-Pads

Pads are small areas of copper in prescribed shapes. Anti-pads are small areas in prescribed shapes where copper is removed. Pads are used both with vias and as exposed outer-layer copper for mounting of surface-mount components. Anti-pads are used mainly with vias.

Since plated through-hole vias are conductive over the whole length, a method is needed to selectively making electrical connections to traces, planes and planelets of the various layers of a PCB. This is the function of pads and anti-pads.

For a via to make a solid connection to a trace on a PCB layer, a pad must be present for mechanical stability. The size of the pad must meet drill tolerance/registration restrictions.

Anti-pads are used in a similar capacity but in reverse. Since plane and planelet copper is otherwise uninterrupted, any via travelling through it makes an electrical connection to it. Where vias are not intended to make an electrical connection to the planes or planelets passed through, an anti-pad removes copper in the area of the layer where the via penetrates.

Lands

For the purposes of soldering surface mount components, pads on outer layers are typically referred to as lands or solder lands. Making electrical connections to these lands usually requires vias. Due to manufacturing constraints of PTH technology, it is rarely possible to place a via inside the area of the land. Instead, this technology uses a short section of trace connecting to a surface pad, and minimum dimension specifications exist defining the minimum length of the connecting trace. Microvia technology is not constrainted and vias can be placed directly in the area of a solder land.

Dimensions

The major factors defining the dimensions of the PCB are FPGA package geometries, PCB manufacturing limits, and system compliance. Other factors such as Design For Manufacturing (DFM) and reliability impose further limits, but as these are application specific, they are not covered here.

The dimensions of the FPGA package, in combination with PCB manufacturing limits define most of the geometric aspects of the above structures, both directly and indirectly. This in itself constrains the PCB designer significantly. The package ball pitch (1.0 mm for FF packages; 0.8 mm for SF packages) defines the land pad layout. The minimum surface feature sizes of current PCB technology define the via arrangement in the area under the device. Minimum via diameters and "keep-out areas" around those vias defined by the